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Article

An Exclusive Switching Performance: Power Factor Correction in Hybrid Modular Multilevel Converter

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A B S T R A C T

This article is devoted to the multi-level inverters and in particular to the switching and Power Factor Correction (PFC) of Hybrid Modular Multilevel Converter (HMMC). The HMMC is built up by individually controllable sub-modules (SMs). Therefore the converter can act as a controllable voltage source converter with a large number of discrete voltage steps. Various Pulse-Width Modulation (PWM) switching processs which are based on a single reference waveform are developed / proposed for the MMC. Active filtering of electric power consumes now develop a mature technology for harmonic mitigation and PFC in ac power networks with nonlinear loads. This paper presents an exclusive switching process which is also helpful to maintain the Power Factor (PF) of HMMC.

Keywords: HMMC, Switching Processs, PFC etc.

Introduction

The Prefabricated Multilevel Converter (MMC) has industrialized the biggest well looked multilevel converter topology for medium/ high-power presentations, exactly for Voltage Source Converter (VSC). MMCs are fabricated up by an amount of fuzzy, but independently wieldy SMs. The SMs in the MMC can either be two-level half-bridge converters, each capable of producing +V or zero voltage, or two-level full-bridge converters, producing ±V or zero voltage.[1] This means that the converter performances as a controllable voltage source with a high number of possible discrete voltage steps. The multilevel topology prevents generation of any major harmonic content.[2] In contrast with additional multilevel converter topologies, the outstanding topographies of the MMC includes: 1) its modularity and scalability to meet any voltage level necessities, 2) its high efficiency, which is of momentous prominence for high-power submissions, 3) its larger harmonic presentation, definitely in high-voltage applications where a big amount of identical SMs with low-voltage ratings are stacked up, in that way the size of passive filters can be abridged, and 4) absence of dc-link capacitors.

Power electronic devices grounded converters offers higher efficiency, compact size and better controllability. But on the other side, due to switching actions, these systems behave as non-linear loads and familiarize harmonics to the DC lines. Active power filter technology is the well-organized way to compensate reactive power and cancel out these generated low order harmonics.

The rest of this paper is prearranged as follows. Section II presents the MMC topology. This is surveyed by an evaluation of latest contributions on MMC modulation processs presented in Section III. The concluding remarks are presented in Section IV.

MMC Topology

Fig. 1 shows a illustration of a three-phase MMC. It consists of two arms per phase leg where each arm contains of N series-connected, identical SMs and a series inductor Lo. The SMs in each arm are skilful to produce the obligatory ac phase voltage; the arm inductor suppresses the high-frequency components in the arm current. The upper (lower) arm of three phase-legs is considered by subscript "p" ("n"). The SMs of the MMC of Fig. 1 can be understood by the succeeding circuits: 1) The half-bridge circuit or chopper-cell[3]: As given away in Fig. 2(a), the output voltage of a half-bridge SM is whichever equivalent to its capacitor voltage Vc (switched on/inserted state) or zero (switched-off/bypassed state), contingent on the switching states of the admiring switch pairs, i.e., S1 and S2. This topology do not offers the DC fault treatment capacity of MMC.

2) The full-bridge circuit or bridge-cell [3]: As depict in Fig. 2(b), the output voltage of a full-bridge SM is one or the other equal to its capacitor voltage Vc (switched-on/inserted state) or zero (switched-off/bypassed state), contingent on the switching states of the four switches S1 to S4. Meanwhile the number of semiconductor devices of a full-bridge SM is twice of a half-bridge SM, the power losses as fit as the cost of an MMC established on the full-bridge SMs are suggestively higher than that of an MMC based on the half-bridge SMs [3]. This topology includes the DC fault handling capacity but necessitates the big amount of switching devices and hence - 1) increases the switching losses 2) additional complex switching process 3) introduces more harmonics. To overcome the demerits of the same, new topology of MMC, fig. 3, is introduced titled as Hybrid Modular Multilevel Converter (HMMC) which offers all the merits of full-bridge SM based MMC as well as requires less number of switching devices and hence - 1) decreases the switching losses 2) less complex switching process 3) introduces less harmonics.

The proposed process for switching of HMMC is applied by using Matlab Simulink platform.

Let N is the no. of SMs per phase out of which F are the FBSMs, noted as $SM_{f(1)}$ to $SM_{f(F)}$. So (N-F) will be HBSM, noted as $SM_{h(1)}$ to $SM_{h(N-F)}$. HBSM generates 0 & Vc voltage levels while FBSM generates 0, Vc & -Vc voltage states. Thus the range of generated total arm voltage is from 0V to . The DC and AC voltages are-

V_{DC} = N.Vc &

V_{an_peak} = ½ * N.Vc = ½* V_{DC}

Now if M FBSMs out off F are allowed to generate –Vc state in each phase (M<F), then the arm voltage range extends between .

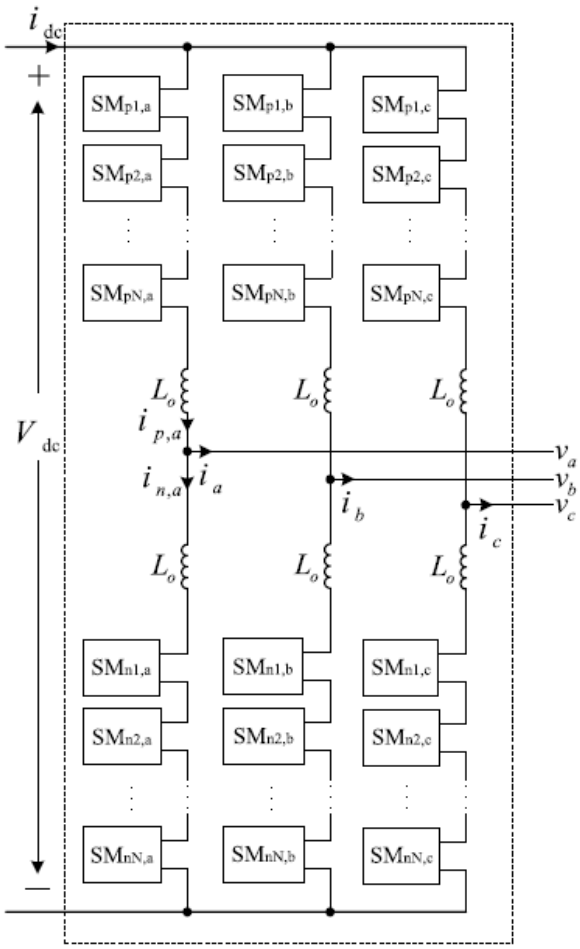

Figure 1.Schematic Representation of MMC

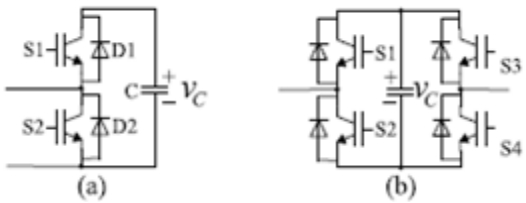

Figure 2.SM topologies: (a) the half-bridge (b) the full-bridge

Under this condition, the DC and peak AC phase voltages are-

V_{DC} = N.Vc – M.Vc

= (N-M).Vc

V_{an_peak} = ½* (N+M).Vc

= ½*V_{DC} + M.V_{DC} / (N-M)

Thus, the peak AC phase voltage can be extended due to M-FBSMs generating the –Vc states

On a Condition, that the series voltage designed by all FBSM capacitors alongside a fault current path is advanced than the AC line to line voltage, a DC fault can be unnavigable

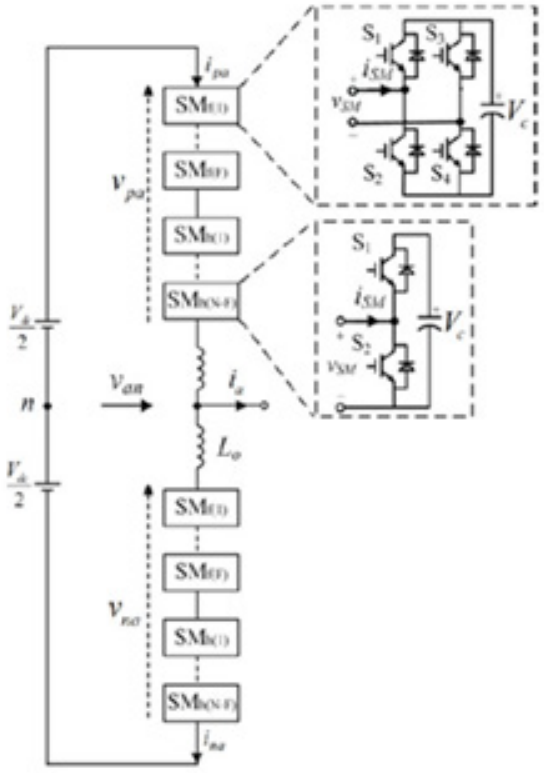

Figure 3.Schematic representation of HMMC

once all the IGBTs are switched OFF. For this necessity, the minimum no. of FBSMs inside each arm can be consequent as-

$$V_{an\_peak} = ½^* (N+M).Vc$$
$$= ½^*V_{DC} + M.V_{DC} / (N-M)$$

the peak line to line AC voltage for the MMC during a DC fault is

$$Vmax = \sqrt{3} * \frac{(N+M)}{2(N-M)} * Vdc$$

All arm has F no. of FBSM, therefore the arm voltage made by the FBSMs through DC fault is-

$$Varm = F * Vc = \frac{F}{(N-M)} * Vdc$$

The blocking voltage shaped by two series arm voltages (one upper arm and one lower arm in different legs) and the AC line to line voltage would meet the subsequent measures-

$$Vmax = \frac{\sqrt{3}(N+M)}{2(N-M)} * Vdc \leq \frac{2F}{(N-M)} * Vdc = 2Varm$$

Thus, for positively block DC faults, the whole no. of FBSMs has to meet the succeeding condition-

$$F \geq \frac{\sqrt{3}}{4} * (N+M)$$

Switching Processs Of The MMC

Switching Processs

Various pulse-width modulation (PWM) process, constructed on using a single reference waveform, that have been established/ proposed for the switching of MMC includes:

Table 1.Comparison of Various Mmc Topologies

Parameters	HBMMC	FBMMC	Hybrid MMC	
			M=0, F = ½*N	M = 1/3*N, F = 2/3*N
DC Link Voltage	V_{DC}	V_{DC}	V_{DC}	V_{DC}
Max. AC Volt.	½*V_{DC}	½*V_{DC}	½*V_{DC}	V_{DC}
SMs / phase	4n	4n	4n	6n
IGBTs / phase	8n	16n	12n	20n
Diodes / phase	8n	16n	12n	20n
DC fault Blocking	No	Yes	Yes	Yes

1) Carrier-disposition PWM development (CD-PWM) [4],

[5]: These procedure require N identical triangular carrier waveforms expatriate proportionally with respect to the zero axis. The contrast of the phase voltage reference waveform with the carriers constructs the anticipated switched output phase voltage level.

Voltage transitions consistent to a triangular carrier are related with the insertion/bypass of a specific SM. Grounded on the phase shift among the carrier waveforms, these development are extra categorized into: a) phase disposition (PD), b) phase opposition disposition (POD), and c) alternate phase opposition disposition (APOD), depict in Fig. 4(a)–(c), correspondingly.

The technical hitches of by means of these enlargement comprise unsatisfactory distribution of voltage ripple across the SM capacitors that influence the harmonic distortion of the ac-side voltages and large magnitude of circulating currents. To early payment the harmonic distortion of the ac-side voltages, an unassuming carrier rotation process [6], a improved carrier rotation method [7], or a signal rotation process [4] is castoff to equilibrium the voltage distribution across all the SM capacitors.

In meanness of the planned SM capacitor voltage corresponding process, the output voltages have a comparatively high total harmonic distortion (THD).[4] To upsurge the enactment of these process, a modified PD PWM procedure with an SM capacitor voltage balancing process is planned in.[8]

In this development, which is established on the PD carrier waveforms, voltage transitions conforming to a triangular

carrier are no lengthier dispensed to a precise SM. In this course, assessment of the orientation waveform with the carrier waveforms produces an (N + 1)-level waveform that defines the number of SMs to be inserted in the upper and lower arms, respectively. Depending upon the direction of the arm current and the status of the SM capacitor voltages, the determined number of SMs out of the N SMs in the upper (lower) arm are introduced so as to minimalize the modification between the SM capacitor voltages.

Mei et al. in[9] suggest a PD PWM method with discriminating loop bias mapping process for complementary the SM capacitors. This process outfits carrier rotation by means of the subsequent feedback: a) the maximum/minimum SM capacitor voltages and b) the direction of arm current. The benefits of this performance comprise: a) nonappearance of additional orientation signals to control the SM capacitor voltages and b) ease of execution in a modest field applied gate array (FPGA) even with a great amount of SMs.

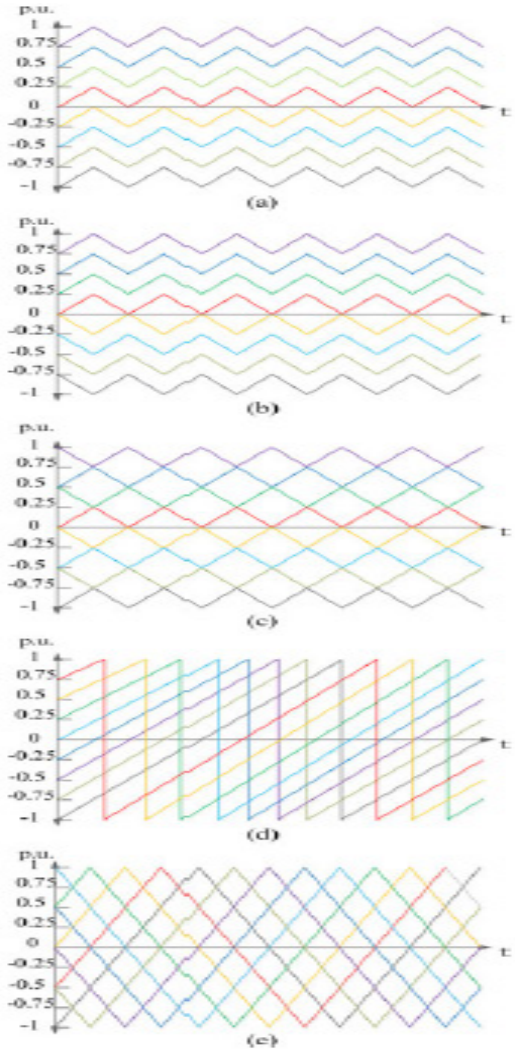

Figure 4.Multilevel carriers: (a) PD, (b) POD, (c) APOD, (d) saw-tooth, and (e) phase-shifted carriers

Subharmonic processs[4]: In these processs, there are 2N identical carrier per phase-leg, either sawtooth waveforms or triangular waveforms, with a phase shift of θ = 360^0/2N with respect to each other, as depict in Fig. 4(d) and (e). Assuming the same number of switching transitions for both the PD PWM and subharmonic development, the PD PWM development produces better line-to-line voltage THD.

Furthermore, there are numerous modulation process constructed on by means of multiple orientation waveforms. These modulation process comprise:

Direct modulation: In this modulation process, the upper and lower arm voltages of phase-j are controlled by two harmonizing sinusoidal orientation waveforms, as given by

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} - v_{j,ref}}{V_{dc}}$$

$$n_{n,j,ref} = N\frac{\frac{V_{dc}}{2} + v_{j,ref}}{V_{dc}}$$

where Vj,ref characterizes the reference output voltage and $n_{p,j,ref}$ and $n_{n,j,ref}$ are the reference waveforms for the number of introduced SMs in the upper and lower arms, respectively. The orientation waveforms in (1) are related with the PD carrier waveforms, which vary among 0 and N, to control the obligatory number of inserted SMs in the upper and lower arms. The foremost shortcoming of the direct modulation process is the amount of circulating currents, which escalation the converter power losses and rating values of the components.

2) Indirect modulation: In this procedure, the upper- and lower-arm orientation waveforms of phase-j are given by

$$n_{p,j,ref} = N\frac{\frac{V_{dc}}{2} - v_{j,ref} - v^{\Sigma}_{reg,j} - v^{circ}_{reg,j}}{\Sigma^{N}_{i=0} v_{cp,i,j}}$$

$$n_{n,j,ref} = N\frac{\frac{V_{dc}}{2} + v_{j,ref} - v^{\Sigma}_{reg,j} - v^{circ}_{reg,j}}{\Sigma^{N}_{i=0} v_{cn,i,j}}$$

wherecharacterises the capacitor voltage of SM-i in arm-x of phase-j, and andare used to control the total energy in the phase-j leg and equilibrium the energy between the arms, consistently. Comparable to the direct modulation development, the reference waveforms are compared with the PD carrier waveforms to determine the number of inserted SMs in the upper and lower arms.

Phase-shifted carrier-based PWM process (PSC PWM)[19]: In this development, each SM of the MMC is controlled self-sufficiently, and the voltage balancing task of the SMs is divided into an averaging control and a balancing control. The orientation waveforms of each SM in the upper and lower arms are prearranged by

$$m_{p,i,j} = \frac{\frac{V_{dc}}{2N} - \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cp,i,j}}$$

$$m_{n,i,j} = \frac{\frac{V_{dc}}{2N} + \frac{v_{j,ref}}{N} + v_{a,j} + v_{b,i,j}}{v_{cn,i,j}}$$

where $V_{a,j}$ and $V_{b,i,j}$ are the averaging and balancing controller outputs, respectively. The averaging and balancing methods control the average SM capacitor voltage in each phase-leg and the separate SM capacitor voltage, correspondingly. Comparison of each SM voltage reference waveform with its triangular carrier produces the switching signals for the conforming SM. The triangular carrier waveforms of every phase-leg are executed based on the sub-harmonic process. The chief shortcomings of this progression are its application effort that meaningfully upsurges as the number of SMs intensifications and unpredictability under certain functioning conditions.

Table 1.Comparison of Modulation Strategies

Property	Modified PD-PWM	Direct Modul-ation	Indirect Modul-ation	PSC-PWM
No. of ref. waveforms	1	2	2	2N
Additional Controllers required for Stability	No	No	Yes	Yes
Presence of circulating Current	Yes	Yes	No	No
Implemen-tation Effort	Moderate	Moderate	Low	High

A brief comparison of the aforementioned modulation strategies is provided in Table II.

SHE–PWM method is planned in [11], in which the switching patterns are strong-minded to remove the low-order harmonics of the output voltage waveform. The switching patterns are planned and stored in lookup tables for various modulation indices and the output-voltage phase angle.

A Nearest Level Control (NLC) modulation development is suggested in,[12] in which the voltage level nearest to the desired voltage waveform is selected. Compared to the SHE–PWM, the NLC process is easy to implement, necessitates less computational efforts, and uses a lower switching frequency when compared to the PWM processs. The expansion proposed in [13] optimizes the pulse patterns to diminish the harmonic distortion of the output voltage. The main compensations of fundamental frequency switching process are the concentrated switching frequency and low THD of the output voltage deprived of any limitation on the output-voltage frequency. This leftovers opposed to the PWM process where the carrier frequency imposes a limit on the output-voltage frequency.

Exclusive Switching Process: This control can be useful for HBSM as well as FBSM. The switch, S_1 is turned on at ωt = (π−β)/2 and then turned off at ωt = (π+β)/2 . The other switch, S_2 is bowed on at ωt = (3π−β)/2 and then turned off at ωt= (3π+β)/2 . The output voltage is varied by varying conduction angle, β. The gate signals are produced by comparing triangular wave with a dc signal as represent in Fig.5. The fundamental component of input current is in phase with input voltage, and the displacement factor is unity (1.0). Consequently, the power factor is better-quality.

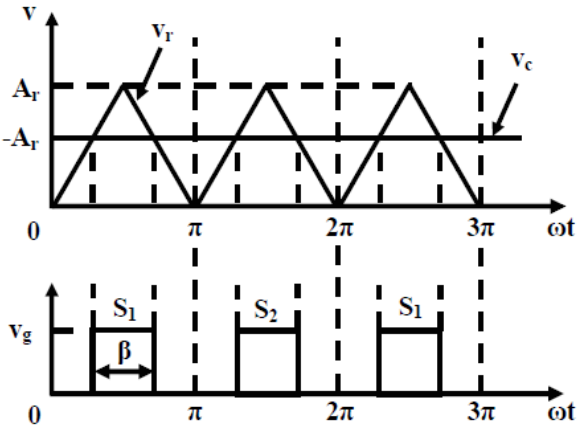

Figure 5.Exclusive Switching Process

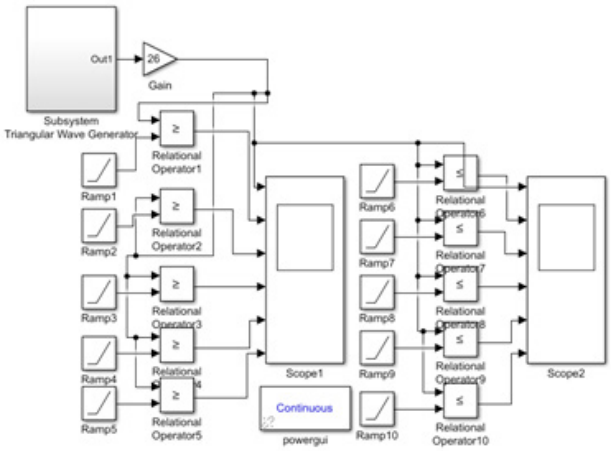

Figure 6.Generation of Gate Signals

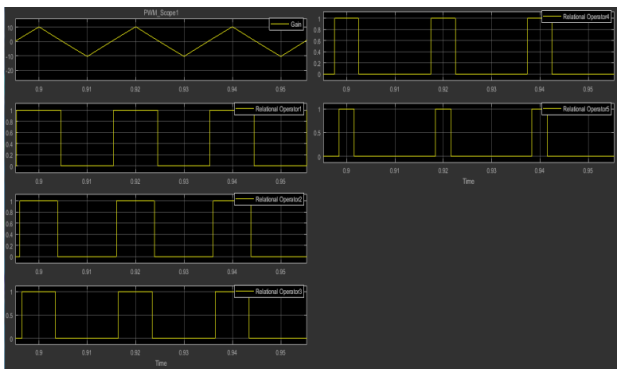

Figure 7.Gate Signals for Upper SMs

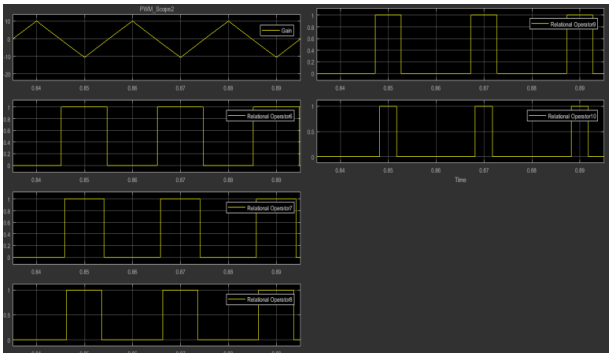

Figure 8.Gate Signals for Lower SMs

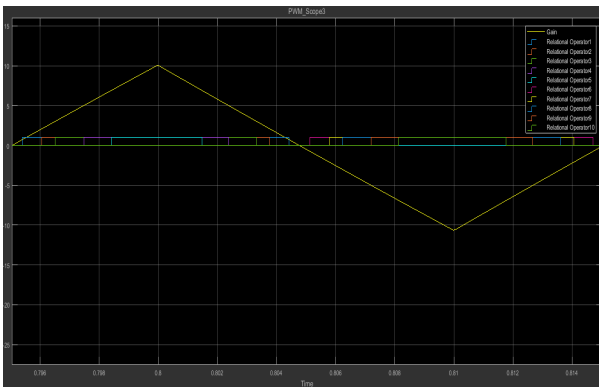

Figure 9.Gate signals for all SMs in one ARM

Conclusion

With a noteworthy amount of MMC-derived converter topologies and uses, it is single-minded that growth of novel modulation and control strategies will be a foremost driving factor to shape the future of MMC uses.

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