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Efficient Design Strategies for Low Power and Area in VLSI Circuits

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A B S T R A C T

Leakage power, which accounts for an ever-increasing fraction of chip overall power consumption in deep submicron technologies, is crucial for a low power design. When designing CMOS VLSI circuits, power dissipation is a crucial factor. In battery-powered applications, high power consumption reduces battery life and has an impact on packing, cooling, dependability. We provide a method for constructing CMOS gates dubbed LCPMOS that considerably reduces leakage current without raising dynamic power dissipation. Leakage power is essential for a low power design since it represents an ever-increasing portion of the overall chip power consumption in deep submicron technologies. Power dissipation is an important consideration while building CMOS VLSI circuits. High power consumption affects reliability, cooling, packaging, battery life in applications that use batteries. We provide the LCPMOS approach, which significantly lowers leakage current without increasing dynamic power dissipation, for building CMOS gates. A single additional leakage control transistor, driven by the output from the pull up and pull down networks, is used in LCPMOS, a technique to address the leakage issue in CMOS circuits. It is placed in a path from the pull down network to ground and provides the additional resistance, reducing the leakage current in the path from supply to ground.The primary advantage over other systems is that the LCPMOS technology doesn't need any additional control and monitoring circuitry, hence reducing the active state power consumption and constricting the active state area. Along with this, another benefit of the LCPMOS approach is that it decreases leakage power to a level of 91.54%, which is more effective than other leakage power reduction techniques in terms of area and power dissipation.

Keywords: Sub Threshold Leakage Current, LCPMOS, Voltage Scaling, LCT, Self-Controlled LCT, Deep-Submicron

Introduction

The three main causes of power loss are leakage current, short-circuit currents, capacitive power loss caused by load capacitance charging and discharging. Short-circuit currents are generated when a logic gate briefly creates a conducting path between the voltage supply and ground. Subthreshold currents and reverse-bias diode currents make up the leakage current. According to Figure 1, the former is caused by the stored charge between the source and drain of active transistors, whereas the latter is caused by carrier diffusion between the source and drain of OFF transistors. In today's

world, digital integrated circuits are everywhere, many of them are found inside of mobile devices that have a limited amount of power (such as mobile computers, watches, phones). Such devices must be created to consume the least amount of power possible in order to allow a usable battery runtime. Low power consumption is particularly crucial for non-portable equipment. The dependability of the circuit, which is closely related to the operating temperature of the circuit, can be greatly increased and the packaging costs can be significantly decreased by reducing the power consumption. Low power consumption is thus a zero-order restriction for the majority of ICs produced today. . In fact, today's manufacturers of microprocessor chips have adopted the motto of better performance-per-watt.The feature size and threshold voltage of CMOS technology have been decreasing for decades in order to achieve high density and high performance. Transistor leakage power has rapidly increased as a result of this tendency. The requirement to maintain a steady electric field on the ever-shrinking gate oxide drives the reduction in supply voltage. Unfortunately, in order to maintain an acceptable transistor speed (proportional to the transistor "on" current), the threshold voltage must also be decreased, which causes the "off" transistor current—the current that constantly flows through the transistor even when it should be "non-conducting"—to exponentially increase.

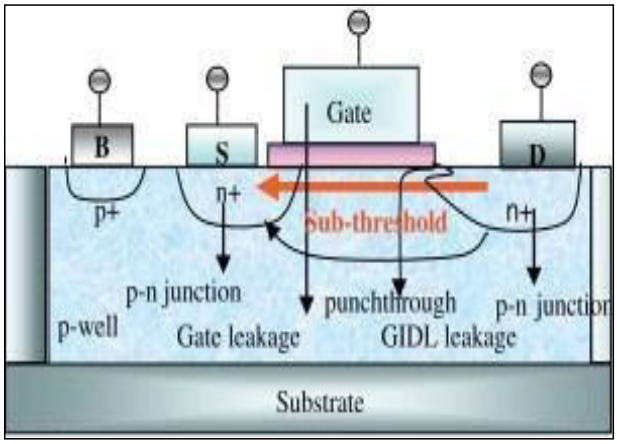

Figure 1.Static CMO Sleakage sources.

Shorter channel lengths cause an increase in sub-threshold leakage current through a transistor when it is off as the feature size decreases, as demonstrated in fig2. Due to the fact that transistors cannot be entirely turned off, low threshold voltage also causes an increase in sub-threshold leakage current. Due to these factors, leaky power dissipation, also known as static power consumption, has grown to represent a sizeable fraction of overall power consumption for present and future silicon technologies. Numerous researchers have put forth various solutions for the power dissipation issue, ranging from device-level solutions to architectural solutions and beyond.

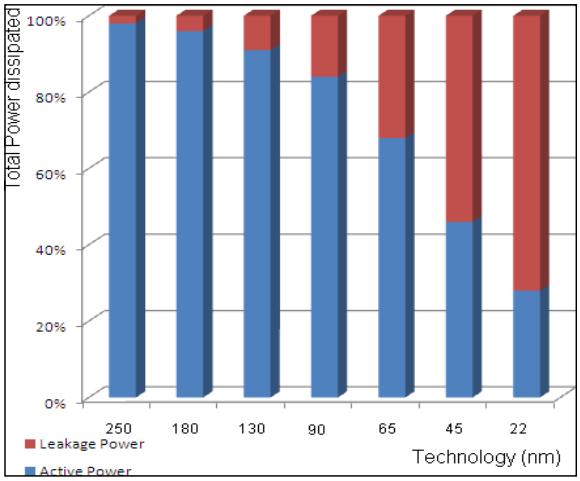

Figure 2.Technology Vs Leakage Power

As the size of the feature shrinks, the sub-threshold leakage current through a transistor rises when it is off, as seen in Figure 2. This rise is also brought on by shorter channel lengths. Sub-threshold leakage current increases when threshold voltages drop because transistors cannot be completely turned off at such low levels. Because of these considerations, static power consumption—also known as leaky power dissipation—has grown to represent a sizeable portion of the total power consumed by current and emerging silicon devices.Many academics have proposed a variety of answers to the power dissipation problem, from device-level answers to architectural answers and beyond.

Limitations with Related Work

One. MTCMOS

Between the pull-down network and the ground, a high-threshold NMOS gating transistor is linked, low-threshold voltage transistors are employed in the gate.The presence of reverse conduction channels tends to diminish the noise margin or may cause the gate to completely fail. The high-threshold transistors connected in series with all the switching current channels also have an impact on performance.

A variation of MTCMOS known as the dual VT method uses high-threshold transistors for gates in the non-critical path and low-threshold transistors for gates in the critical path.[3,7] For each value of VT during fabrication, both approaches call for additional mask layers, which complicates the work of depositing two distinct oxides of varying thickness and adds to the complexity of the manufacturing process. The methods also experience turning-on latency, which means that after reactivating an idle circuit, it takes some time for it to recover to its regular working state. For the former method, the delay is normally a few cycles, however for Dual technology, it is substantially higher.These methods are ineffective at reducing leakage power when the circuit is active.

SIEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-

Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width.[6] Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turnedoff. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time

Zigzag Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

Sleepy Stack Technique

This technique combines the structure of the Forcedstack technique and the sleeptransistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor[10]. Although using of W0/2 for the width of the sleeptransistor, changing the sleep transistor width may provide additional tradeoffs between delay,power and area.It also requires additional control and monitory circuit,for the sleep transistors.

Leakage Feedback Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is drivenby output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

Sleepy Keeper Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuitis active.[9] The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state

Lector Technique

This technique consists of two self controlled transistors which increases the resistance in the path from source to ground, which increases the area of the circuit, one of the mostimportant constraint in the design of vlsi circuits. In the suggested method, a single leakage control transistor (LCT) is added within the logic gate, its gate terminal is controlled by the output of the circuit itself. It results in a large reduction in leakage currents by raising the resistance of the path from the pull-down network to ground and, as a result, raising the resistance from Vddto ground. The key advantage of LCPMOS over other approaches is that it doesn't need any additional control or monitoring circuitry, which reduces active state area and power dissipation.

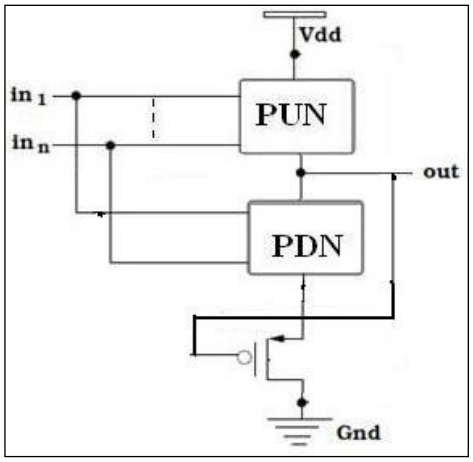

Figure 3.LCPMOSCMOS Gate

Figure 5 depicts the topology of an LCPMOS CMOS gate. Nodes N1 and Gnd are connected by oneLCTs. The output of the circuit itself regulates the LCT's gate terminal. Because the LCT is regulated by output, no external circuit is required, eliminating a drawback of the sleep transistor technology. Leakage current is decreased by the addition of LCT because it raises the resistance of the passage from Vdd to Gnd.

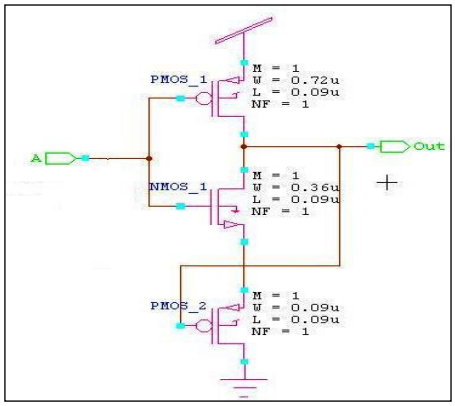

Figure 4.LPCMOS based CMOS Inverter

Leakage ControlPMOS(LCPMOS) technique is illustrated in detail with the case of an inverter. A LCPMOS INVERTER is shown in Figure 6. A PMOS is introduced as LCT between N1 and Gnd nodes of inverter.

WhenV_{dd}=1V, input A=0, the output is high. As the output drives the LCT the LCT goes to OFF state hence provides high resistance path between V_{dd} and Gnd. When A=1,theoutput is low; hence LCT will be in ON state hence output is low. LCPMOS inverter for all possible inputs are tabulated in Table 1.

Table I.State Matrix of LCPMOS inverter

Transistor Reference	InputVector(A)	
	0	1
M1	ONState	OFF State
M2	OFFState	ON State
LCT	Near Cut-OFF State	ON State

The sleep transistors in the sleep-related approach must be able to isolate the power source and/or ground from the other transistors in the gate. They must be made bigger to dissipate more dynamic power as a result. This cancels out the cost savings from the circuit being idle. The input vector is a need for the sleep transistor approach, additional circuitry is required to monitor and manage the switch in the sleep transistors, using power in both the active and idle modes. In contrast, LCPMOS is vector independent and creates the necessary control signals inside the gate. No matter how many transistors are in the pull-up and pull-down networks, LCPMOS method only adds one transistor to each channel from Vdd to Gnd. Forced stack, however, saves 100% of the area overhead. With LCT, there is a continual loading demand, which is substantially less.

Applying ICPMOS to CMOS Circuits

Various circuit applications of the LCPMOS technique are explored in this section. The LCPMOS technique is applied to the following CMOS circuits and also the irrespective basecase are implemented to calculate the amountof leakage power reduced in LCPMOS technique.

LCPMOS based NOT gate

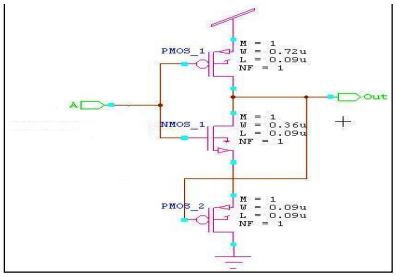

Figure 5.In put LCPMOSNAND

Conclusion

With the advancement of deep-submicron and nanometer technologies, the increase in leakage power caused by the lowering of supply and threshold voltages in order to achieve high performance and low dynamic power dissipation becomes more pronounced, making it much more difficult to address the issue. One LCT is used in LCPMOS, it is controlled by the circuit output. Since LCPMOS does not need any additional control and monitor circuitry and also maintains the exact logic state, it has the advantage of not affecting dynamic power compared to other leakage reduction techniques like LECTOR, sleepy stack, sleepykeeper, etc. When used with general logic circuits, the LCPMOS approach reduces leakage by up to 80–92% compared to the corresponding traditional circuits without compromising dynamic power.Here, there is a trade-off between area overhead and propagation latency.

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