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Research Article

Powering the Future: Emerging Paradigms in Low-Power VLSI Design

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A B S T R A C T

This study surveys the recent trends in the innovations and advancements in the field of low power VLSI Design. Although Low Power is a well-established field, it has seen several advancements, including adiabatic logic. Other advancements include transistor sizing, process shrinkage, voltage scaling, clock gating, etc. The purpose of this paper is to discuss recent developments in low power design.

Keywords: Multi Threshold, Dynamic Voltage And Frequency Scaling, Split Level Charge Recovery Logic, Efficient Charge Recovery Logic

Introduction

Although there are many distinct types of power consumption, dynamic power and leakage power are the main types that have an impact on CMOS circuits.[1]

Dynamic power

The power used by a device when it is actively moving from one state to another is referred to as dynamic power[2] or dynamic powe.[3] Internal power, also known as short circuit power, is spent internally by the device while it is changing state. Switching power is used to charge and discharge the loads on a device.

The dynamic power dissipation that can take place in CMOS circuits is depicted in Figure 1.

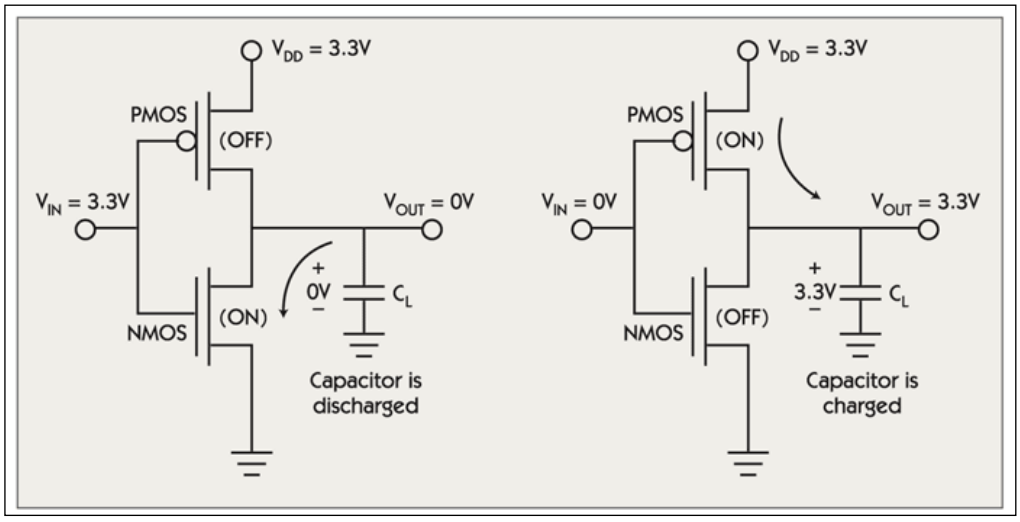

Figure 1.Dynamic power reduction

Leakage power

The power used by a device that is unrelated to state changes is known as leakage power.[2] Although leakage power is used by a device both when it is static and when it is switching, the main concern with leakage power is when the device is in its inactive state because all of the power used in this condition is seen as "wasted" power.[3]

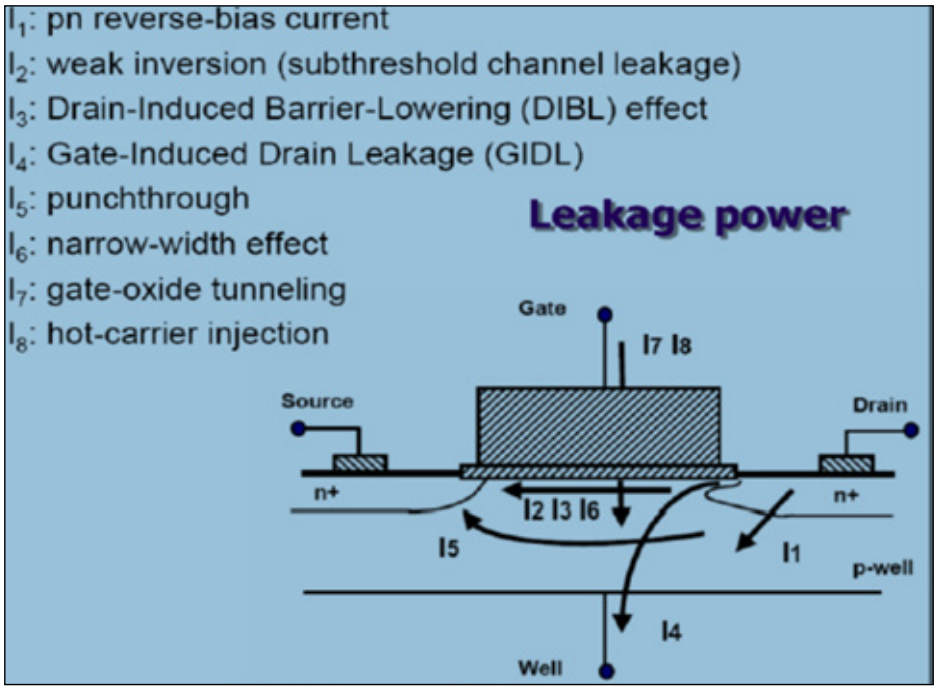

Figure 2.Causes of leakage power

Different causes for the leakage power like reverse bias current, sub threshold channel leakage current,

drain induced barrier lowering leakage, gate induced drain leakage, punch through, narrow width effect,

gate oxide tunneling current, and hot carrier injection current[2] are depicted in Figure 2.

Various techniques have been developed to reduce both dynamic and leakage power. CMOS circuit

dynamic power consumption equation is

P=ACV2FCLK

P stands for the amount of power used, A for the percentage of the circuit that is switching, C for switched capacitance, V for supply voltage, and F for clock frequency. The charge transferred per cycle is CV and the charge moved per second is CVF if a capacitance of C is charged and discharged by a clock signal of frequency F and peak voltage V. Given that the charge packet is given at voltage V, the power, or the amount of energy lost every cycle, is

Power = Capacitive load × Voltage2 × Clock Frequency[5]

Half of the quoted power will be the data power for a timed flip-flop, which can only toggle once every cycle. Their power consumption will be reduced when capacitances are clock gated or flip-flops do not toggle every cycle. Therefore, the average switching activity in the circuit is modelled using a constant known as the activity factor (0A1).

Traditional Power Reduction Techniques

Technology scaling, voltage scaling, clock frequency scaling, switching activity reduction, etc., were frequently employed to reduce this power.

The two most typical conventional, traditional methods are:

Clock Gating

Clock gating is a technique which is shown in Fig. 3 for power reduction, in which the clock is disconnected from a device it drives when the data going into the device is not changing. This technique is used to minimize dynamic power.

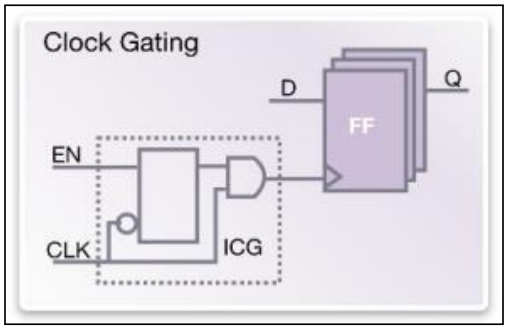

Figure 3.Clock gating for power reduction.

Clock gating is a mainstream low power design technique targeted at reducing dynamic power by disabling the clocks to inactive flip-flops.

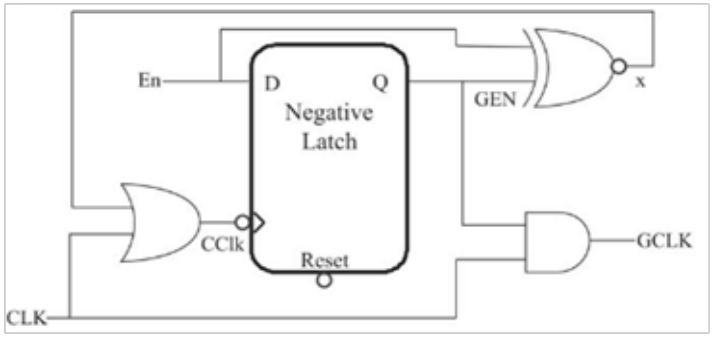

Figure 4.Clock gating for power reduction.

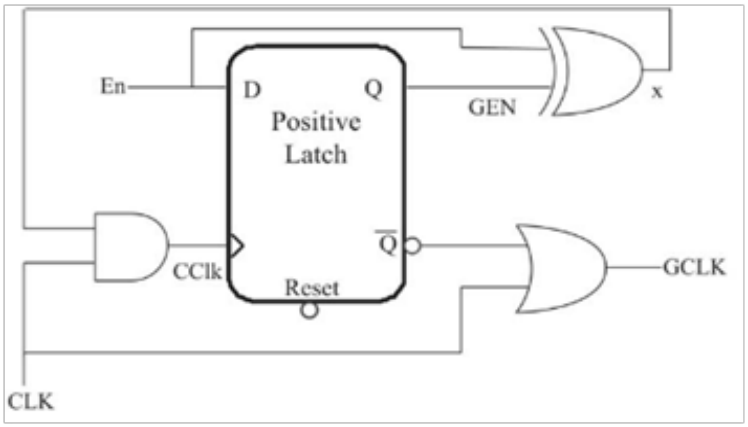

Figure 5.Generation of gated clock when positive latch is used

As seen in Figures 4 and 5, positive or negative latches can also be employed to save additional energy. This conserves energy in such a way that even when the clock on the target device is "ON," the clock on the controlling device is "OFF." The controlling device's clock is also "OFF" when the target device's clock is. Avoiding idling at the clock net can save more electricity in this case.[6]

Multi-Vth optimization/ (Multi Threshold -MTCMOS):

MTCMOS is the replacement of faster Low-Vth (Low threshold voltage) cells, which consume more leakage power, with slower High-Vth (high threshold voltage) cells, which consume less leakage power [7]. Since the High-Vth cells are slower, this swapping can only be done on timing paths that have positive slack and thuscan be allowed to slow down. Hence multiple threshold voltage techniques use both Low Vt and High Vt cells[8]. It uses lower threshold gates on critical path while higher threshold gates off the critical path.[9]

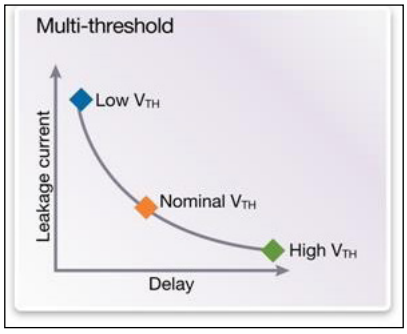

Figure 6.Variation of threshold voltage with respect to the delay and leakage current

Figure 6 shows the variation of threshold voltage with respect to the delay and leakage current. As Vt increases, delay increases along with a decrease in leakage current. As Vt decreases, delay decreases along with an increase in leakage current. Thus an optimum value of Vt should be selected according to the presence of the gates in the critical path. As technologies have shrunk, leakage power consumption has grown exponentially, thus requiring more aggressive power reduction techniques to be used. Several advanced low power techniques have been developed to address these needs. The most commonly adopted techniques today are in below:

- Dual VDD
- A Dual VDD Configuration Logic Block and a Dual VDD routing matrix is shown in Figure 7

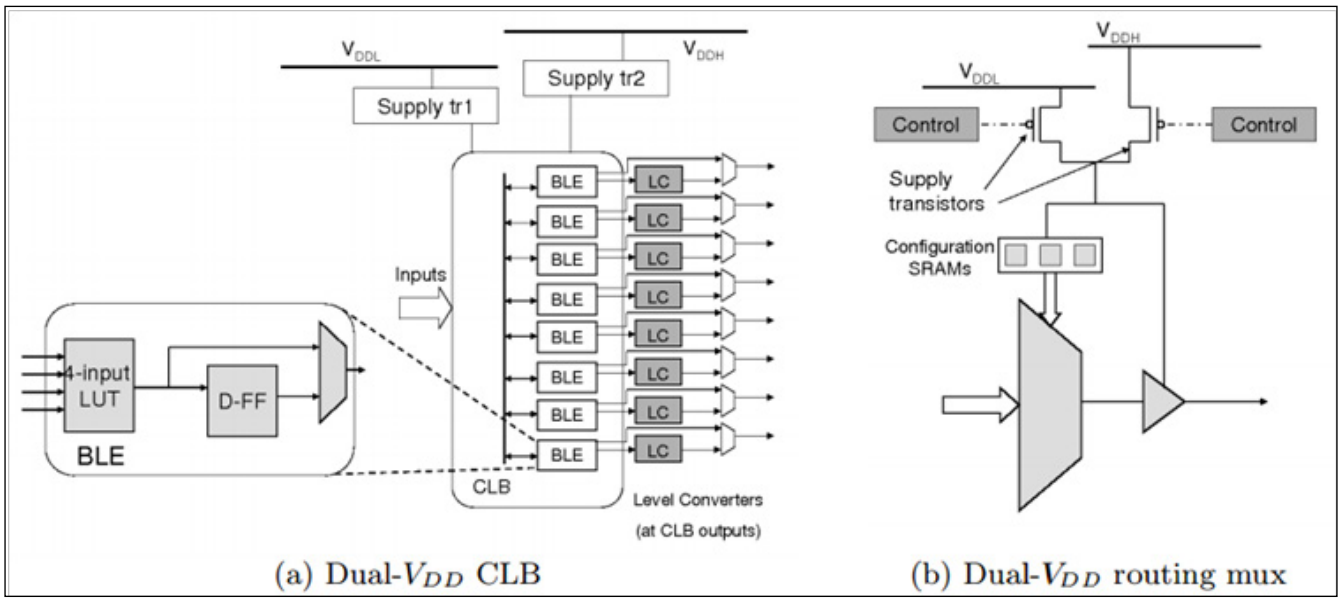

Figure 7.Dual VDD architecture

In the Dual VDD architecture,[10] the logic and routing blocks' supply voltages are programmed to reduce power consumption by assigning low-VDD to design paths that aren't timing-critical while assigning high-VDD to design paths that must meet timing constraints. This is illustrated in Figure 8.

The contact between the VDDL and VDDH parts, however, experiences static current flow if two distinct source voltages coexist. Thus, a low VDD can be up converted to a high VDD using level converters.

Clustered Voltage Scaling (CVS)

This method uses two supply voltages to reduce power without affecting circuit performance.[11] As seen in Figure 9, the critical path's gates are operated at the lower supply to reduce power. The circuits that run at lower voltages are grouped together, resulting in clustered voltage scaling, in order to reduce the number of interfacing level converters required.[11]

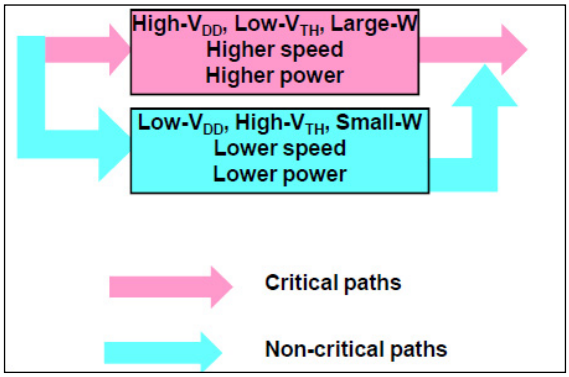

Figure 8.High VDD for critical paths and low VDD for non-critical paths

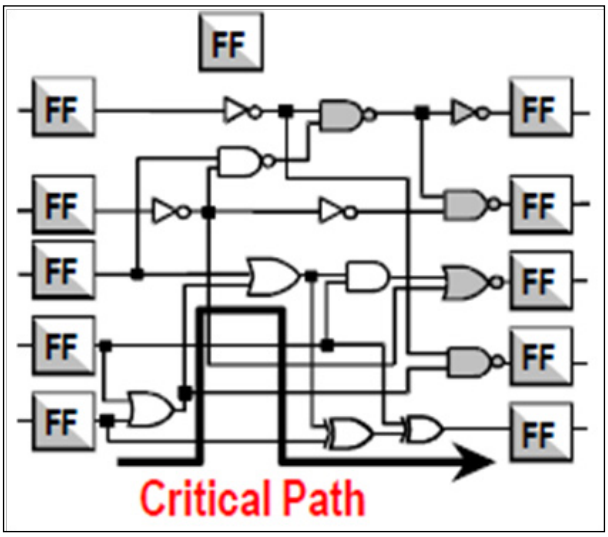

Figure 9.Gates of the critical paths are run at lower supply

Here only one voltage transition is allowed along a path and level conversion takes place only at flipflops.

(3) Multi-voltage (MV) MV is concerned with how various components of a design function at various voltage levels [9]. Only particular sections are connected to the higher voltage supplies in order to achieve performance goals. Significant power savings are made possible by the operation of other components in the system at a lower voltage. Typically, multi-voltage is a technique.

DVFS (Dynamic Voltage and Frequency Scaling)

Dynamic Voltage and Frequency Scaling, often known as DVFS, is the process of changing a device's operating voltage and/or frequency while it is in use so that the least voltage and/or frequency required for a specific mode's proper operation are employed.[12]

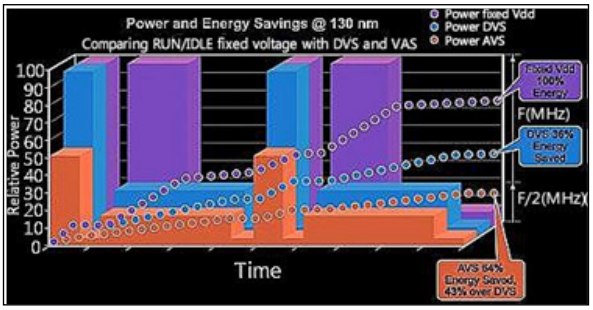

Figure 10.Comparison of fixed voltage, DVS, and AVS energy savings in a processor

AVS is a system-level design that includes parts in the power supply and processor. The AVS loop is controlled by the processor's Advanced Power Controller (APC). The power supply's Slave Power Controller (SPC) receives instructions from the APC and translates them. System integration with the application is made simpler by the IP offered in the APC and SPC, which automatically handle the handshaking required for frequency and voltage scaling.

Adaptive Techniques

Fig. 11 depicts the power and delay dependency on the threshold voltage at 0.5 VDD. It may be deduced from Fig. 11 that Vth must be reduced in order to obtain high performance. However, a reduction in Vth may result in a large rise in the static leakage power component.

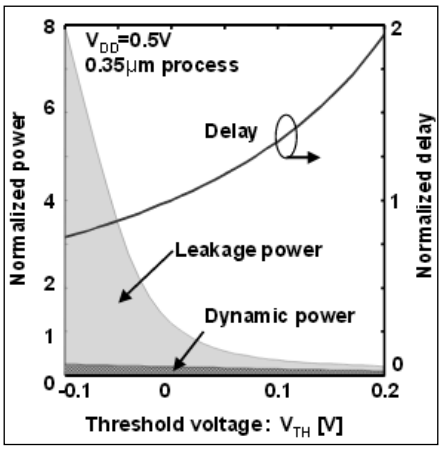

Figure 11.Power and delay dependence on Vth

MTCMOS (Multi Threshold CMOS) and VTCMOS (Variable Threshold CMOS) are two methods for reducing standby leakage current.[11] These strategies are unable to reduce the power of active leakage. Using low Vth transistors solely in the crucial gates, the dual threshold voltage technique divides a circuit into critical and non-critical gates. This scheme's flaw is that the significant leakage current always passes via the low Vth transistors, making it unable to sufficiently suppress the leakage current.

Vth Hopping

Dynamic threshold voltage hopping scheme solves these problems.[15] This scheme utilizes dynamic adjustment of frequency and Vth through back gate bias control depending on the workload of the processor.

When the workload is decreased, less power would be consumed by increasing Vth as depicted in Figure 12. This approach is similar to the dynamic VDD scaling, DVS. In the DVS scheme, voltage and frequency are controlled dynamically based on the workload variation.

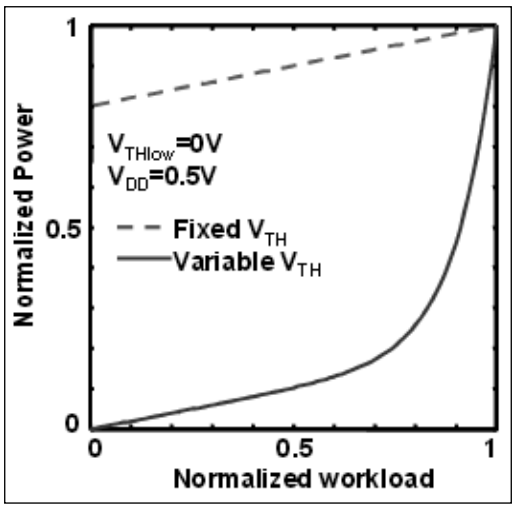

Figure 12.Power dependence on workload

DVS is effective when the dynamic power is dominant. On the other hand, Vth hopping is effective in the low VDD designs, where Vth is low and the active leakage component is dominant in the total power consumption.

Power gating is the complete shut off of supply nets to different areas of a design when they are not needed. Since the power has been completely removed from these shutdown areas, the power for these areas is reduced essentially to zero. This technique is used to reduce leakage power.

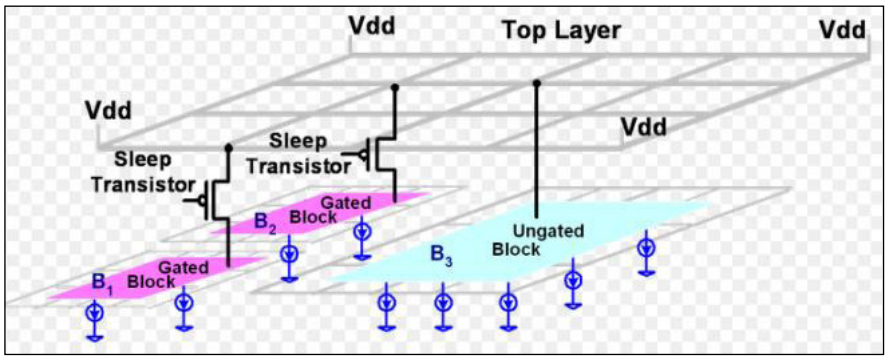

Figure 13.Schematic of a power gating methodology

As seen in Fig. 13, power gating uses high-Vth "sleep transistors" (also known as power switches) to cut off power supply to faster and more powerful circuitry while that logic is not in use. Both header cells, which disconnect the Vdd, and footer cells, which disconnect the Ground, can be used to gate power. Multi-voltage and power gating are frequently used in tandem on the same design, allowing for the operation of several areas at various voltages as well as the ability to shut down one or more of those regions.

Multi-Corner, Multi-Mode (MCMM)

Multi-corner, multi-mode (also known as Multi-Scenario) considers optimization at multiple operating corners, and in multiple operational modes, concurrently, instead of using an iterative process that may never converge.

State Retention

It is the capability to retain the critical state of sequential elements within a block when the block is powered down. State retention generally requires saving the registers and possibly memory contents of the

block.

Well Biasing

Separate voltage supplies can be used to connect to the NMOS and PMOS bulk regions in triple well CMOS

technologies. Modification of these voltages with respect to the primary power and ground supplies is called well-biasing. These supplies can be modulated to provide a back-bias voltage which causes an increase in device Vth, reducing the sub-threshold leakage. These supplies can also be modulated in the reverse direction to provide a forward-bias voltage which causes a decrease in device Vth that increases the speed at which the transistors switch, at a cost of increased sub-threshold leakage. Thus, well-biasing can be used to directly adjust between high performance and low power consumption.

Reduction of Clock Frequency

As IC circuits have gotten smaller, processors have been able to boost clock frequency to run quicker. Although a faster clock improves performance, it also uses more electricity. In order to save power, the clock can be turned off or slowed down anytime there is extra CPU time available. Many CPUs are equipped with circuitry that allows you to change the clock's frequency or even turn it off (in "Sleep mode").

Even with the clock turned off, certain static power reductions will still be necessary in order to save the values in the registers and volatile RAM memory and allow the device to wake up without performing a complete reboot.The hardware needed to bring up a device from sleep mode is interrupt hardware, which cannot be switched off.

By lowering the clock frequency of the FPGA logic while maintaining acceptable performance levels, hardware accelerators can be used to decrease power. However, in addition to a specific degree of data throughput, some applications also need a quick response time to asynchronous events like interrupts.

Unfortunately, by reducing the system's overall clock frequency, the processor's clock frequency is also reduced, which in turn slows the processor's response time to such occurrences. Therefore, decreasing the processor's clock frequency won't be an option if an application needs a quick CPU response time to asynchronous events. However, by incorporating hardware accelerators, we may still achieve considerable power savings even when a design necessitates quick response time.

A slower clock domain for the hardware accelerators and a faster clock domain for the processor can both be employed. We can minimise overall system power consumption without needing to lower processor clock frequency by introducing hardware accelerators operating at very low clock frequencies to handle the CPU's intensive processing workload. The throughput variation with regard to clock frequency is depicted in Fig. 14. It is evident from Fig. 14 that a constant energy cost per operation can be achieved at the expense of provided throughput as the clock frequency is decreased.

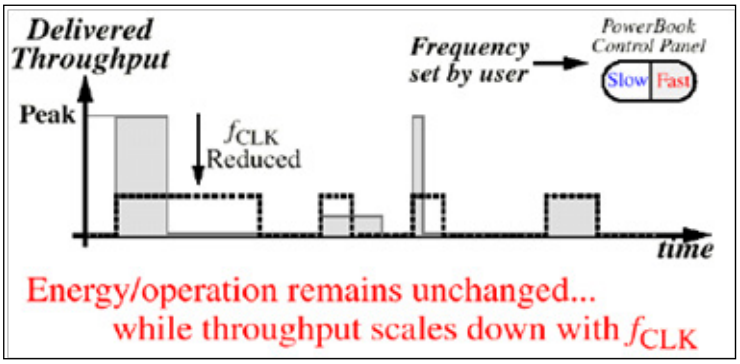

Figure 14.Throughput versus clock frequency

Low Power Buses

In Buses, power consumption takes place by the high capacitance lines and the high switching activities as shown:

$$P = \sum_i \frac{1}{2} \alpha_i f_i C_i V^2$$

Bus Coding-Frequent Value Encoding

This is a technique in which, power dissipation can be reduced by reducing the number of transitions [16]. To minimize the transitions in bus with large capacitance an encoder and a decoder are used as shown in Fig. 15.

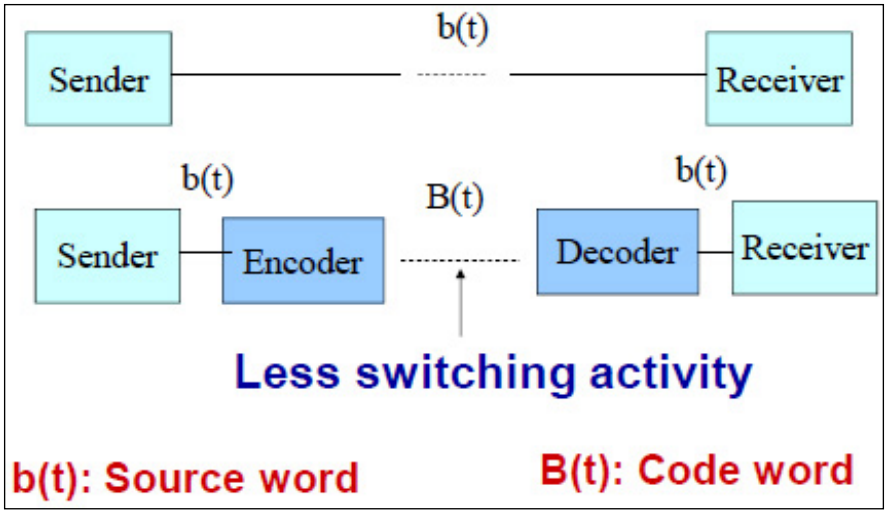

Figure 15.Bus frequent value encoding

Instead of sending the entire data, a coded data is sent for the frequent data, which reduces the switching activity. Otherwise the data is sent unchanged.[17]

Non-Conventional Methods of Low Power Design

Adiabatic Switching

Adiabatic circuits are low power circuits which use “reversible logic” to conserve energy. Unlike

traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules:[18]

1) Never turn on a transistor when there is a voltage potential between the source and drain.

2) Never turn off a transistor when current is flowing through it.

To meet today’s power requirement, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design [19]. During the recovery phase energy will be restored to the power clock, resulting in considerable energy saving.

These include only turning switches on when there is no potential difference across them, only turning switches off when no current is flowing through them, and using a power supply that is capable of recovering or recycling energy in the form of electric charge. To achieve this, in general, the power supplies of adiabatic logic circuits have used constant current charging (or an approximation thereto), in contrast to more traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply. The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors, which store the energy by converting it to magnetic flux. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: “Charge recovery logic”, “Charge recycling logic”, “Clock-powered logic”, “Energy recovery logic” and “Energy recycling logic”. Yet some complexities in adiabatic logic design perpetuate. Two such complexities, for instance, are circuit implementation for time-varying power sources needs to be done and computational implementation by low overhead circuit structures needs to be followed.

Energy recovery circuits face two major obstacles: first, their slowness by today’s standards; second, the fact that they take up about 50% more space than ordinary CMOS and make simple circuit designs more difficult. Charge Recovery Logic (SCRL) at the Split Level Splitlevel Charge Recovery Logic, or SCRL, is a family of adiabatic circuits created by Knight and Younis [20]. The top and bottom rails of this circuit are driven by trapezoidal clocks (1 and / 1) instead of Vdd and ground, which is one of the primary differences between it and the typical NAND circuit depicted in Fig. 16. This distinction is one of the most significant ones.

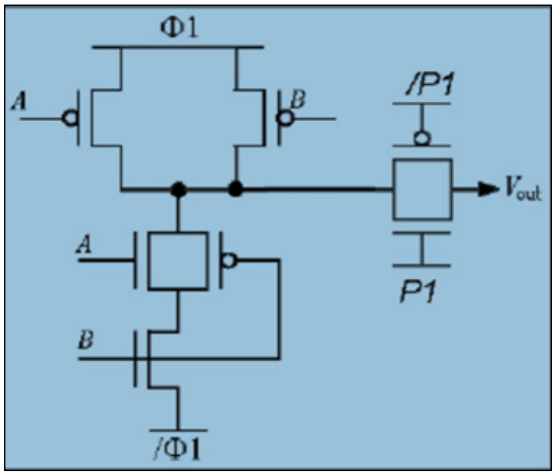

Figure 16.SCRL NAND

The transmission gate is turned off at first because the entire circuit is initially set at Vdd/2 with the exception of P1, which is set to ground, and /P1, which is set to Vdd. The transmission gate is activated in the following phase by progressively changing the values of P1 and /P1. Then, the signals 1 and /, which were at Vdd/2, are split to ground and Vdd, respectively. At this stage, the gate calculates the non-adiabatic NAND of A and B. The transmission gate can be progressively switched back off once the next gate uses the output. When the input has changed, the next cycle can start, and 1 and / 1 are progressively returned to Vdd/2. To avoid breaking the first criterion and turning on a transistor when there is a potential difference, it is crucial to wait to change the input until the rails are back to Vdd/2.[18]

Two Level Adiabatic Logic or 2LAL

The Two Level Adiabatic Logic, also known as 2LAL, was created by Frank and is another intriguing adiabatic circuit family.

This family can be completely pipelined at the gate level, just like SCRL. The fundamental component of a 2LAL is depicted in Fig. 17 by a pair of transmission gates that convey the signals A and A', each of which is symbolised by a single "box" on the left. 2LAL is appropriate for usage with emerging technologies because it doesn't rely on CMOS and simply needs a simple switching device. The fundamental buffer component of a 2LAL is depicted in Fig. 17, which consists of two sets of transmission gates. Both 1 and 0 are trapezoidal clocks, however 1 is one-quarter cycle slower than 0.

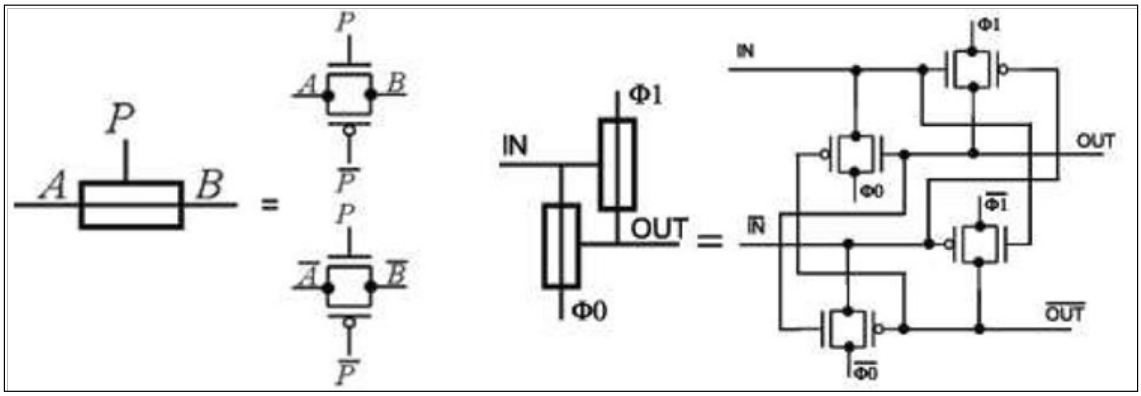

Figure 17.(a) 2LAL basic gate and (b) buffer.

Initially all the nodes are at 0. As the input gradually raises to 1 (if it is 1) or stays at 0, Ø0 transitions to 1.

Quasi Adiabatic Buffers: "Quasi-Adiabatic Logic" refers to logic that uses less power than static CMOS logic while still having certain theoretical non-adiabatic losses. Adiabatic switching with inductors is only possible in systems that use a small number of inductors since high-Q inductors are not readily available in CMOS. By storing recovered energy in capacitors, quasi-adiabatic stepwise charging completely avoids using inductors. On-chip capacitors can be used for stepwise charging (SWC).

Efficient charge recovery logic (ECRL)

Efficient charge recovery logic (ECRL) is proposed as a candidate for low-energy adiabatic logic circuit. Energy recovery process is explained with an inverter example of ECRL (Efficient Charge Recovery Logic inverter) as depicted in Fig. 18. Power supply PC is with trapezoidal pulses [9].

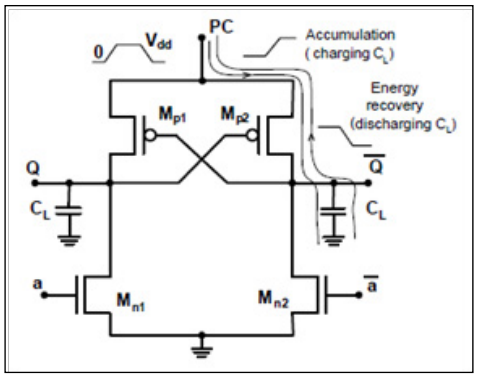

Figure 18.ECRL inverter

The Mn1 is conducting (Q=0) and a=1 in the initial condition. Over conductive transistor Mp2, the output Q follows the change of PC as PC increases from 0 to Vdd. When PC reaches Vdd, it has the criteria Q = 1 and Q = 0, which are acceptable logic states for the next stage's inputs. The right capacitor CL discharges over the conductive Mp2 and PC during the descent of PC from Vdd to zero, recovering collected energy for the PC supply.[21]

Yong Moon and Deog-Kyoon Jeong compare the power consumption of an inverter chain and a carry look-ahead adder (CLA) with that of other logic circuits.[22] For the same throughput as a traditional static CMOS CLA, the ECRL CLA is built as a pipelined structure. The suggested reasoning demonstrates a four to six times reduction in power with a realistic loading and operation frequency range. The suggested supply clock generation circuit uses inductors. 1.0-m CMOS technology with a decreased threshold voltage of 0.2 V is used to design the circuits.

Positive Feedback Adiabatic Logic (PFAL)

Figure 19 depicts the Positive Feedback Adiabatic Logic (PFAL) structure [23]. The logic functions are realised by two n-trees. Additionally, this logic family produces both positive and negative results. The two biggest variations from ECRL are that the functional blocks are parallel with the transmission PMOSFETs and that the latch is constructed by two PMOSFETs and two NMOSFETs rather than just two PMOSFETs as in ECRL [24]. As a result, when the capacitance has to be charged, the corresponding resistance is lower. The chart below shows the relationship between the energy dissipated during a cycle and the energy required for it.

The loaded capacitance transfers energy back to the power source during the recovery phase, resulting in a reduction in the amount of energy being supplied. Positive Feedback Adiabatic Logic (PFAL) is a partial energy recovery circuit construction that exhibits good tolerance to changes in technological parameters [25]. It has two rails, and the adiabatic amplifier, a latch made up of two PMOS and two NMOS, is at the centre of the entire PFAL circuit. This latch prevents the logic level on the output nodes from degrading. The two n-trees free the logic operations.

In order to create a transmission gate, the functional blocks are connected in parallel with P-MOSFETs.

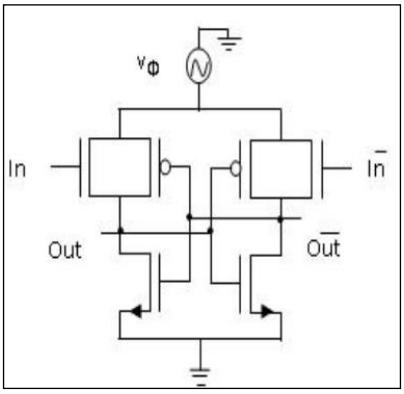

Figure 19.PFAL logic circuit

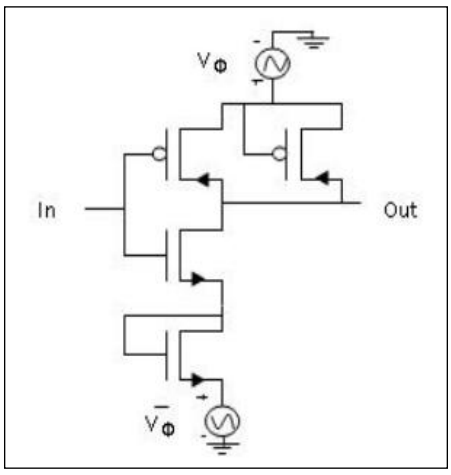

Figure 20.Two phase adiabatic static clocked logic

Phase Adiabatic Static Clocked Logic (PASCL)

The voltage differential between the current-carrying electrodes can be reduced by employing these two split-level sinusoidal waveforms, which have 0.9V peak to peak voltages. As a result, power consumption can be reduced. It makes use of two diodes, one of which is situated between the output node and the power clock, Vclk, and the other of which is situated next to the nmos logic circuit and connected to the other power clock, Vclk. Both diodes are used to increase the pace at which internal nodes discharge by recycling the charge from the output node.

Pre-resolve and Sense Adiabatic Logic (PSAL) Buffer

A innovative quasi-adiabatic logic circuit with a frequency range of 100 KHz to 500 MHz is the pre-resolve and Sense Adiabatic Logic (PSAL) [27]. It uses a differential sensing logic and a big height pre-resolved nMOS structured tree. Because of its low circuit delay, glitch-free output, and reduced switching transients, the logic achieves greater energy efficiency. Improved speed performance is achieved with a significant reduction in switching capacitance. Additionally, the adiabatic pipeline can use less buffers if more than one level of a gate (or a complex gate) is evaluated in each phase. Since four-phase adiabatic logic types are significantly hindered by circuit delay, PSAL improves throughput and reduces critical route length, which in turn improves frequency performance. The incomplete charge-recovery and floating output node issues present in adiabatic logic architectures are overcome by the nMOS structured cascode tree and differential sensing logic.

Recovering Energy Clocking

The input gate capacitances and clock networks are the principal targets of energy recovery techniques. Applying energy recovery techniques to internal nodes could result in a power short-circuit because of the sluggish falling/rising transition of energy recovery signals. When compared to square-wave clocking, the sinusoidal clock technique shown in Fig. 21 can reduce the power related to clock dispersion by more than 90%.

Sinusoidal clock waveforms offer metal-only clock distribution without clock buffers, synchronisation for coarse-

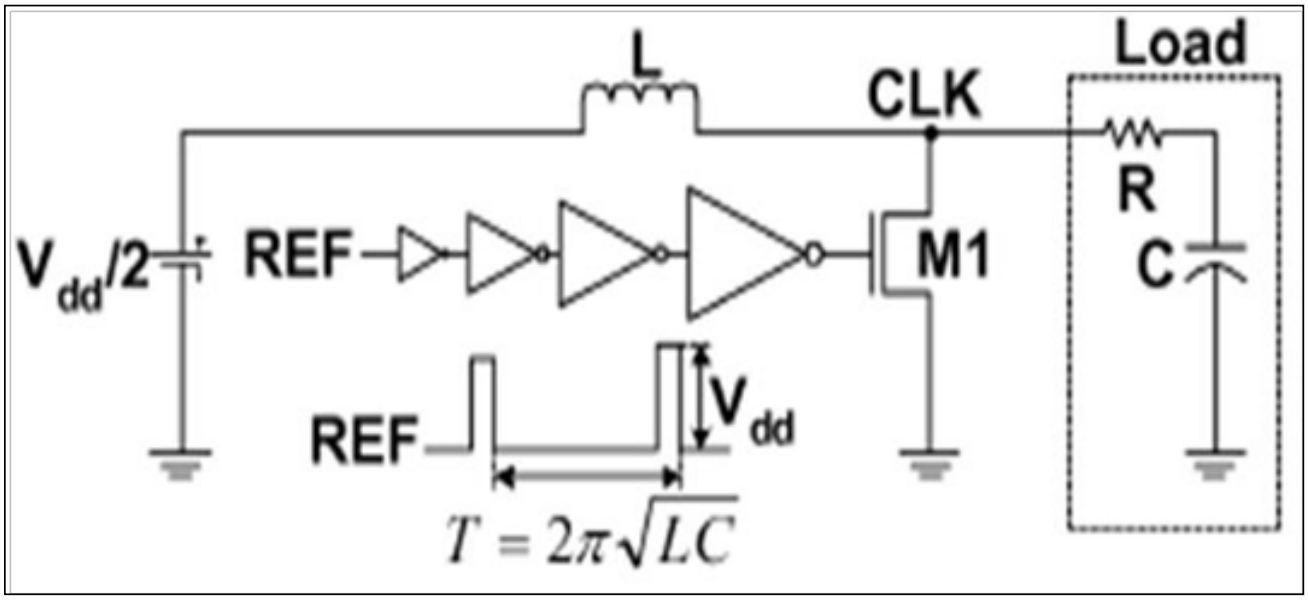

Figure 21.Energy recovery clock.

grain recovery, and synchronisation with power delivery for fine-grain recovery. Additionally, this offers significantly decreased clock uncertainty due to the removal of buffers, significantly decreased clock jitter due to a reduction in the need for clock power replenishment, significantly decreased gate leakage due to lower average voltages across gates, and increased dependability. Additionally, a sinusoidal clock lessens electromagnetic interference.

Asynchrobatic Logic

Asynchrobatic Logic, introduced in 2004, is a CMOS logic family design style using internal stepwise

charging that attempts to combine the low-power benefits of the seemingly contradictory ideas of

"clock-powered logic" (adiabatic circuits) and "circuits without clocks" (asynchronous circuits).

Energy Dissipation Comparison

Fig. 22 shows the comparison of the power dissipation in picoJoules between energy recovery logic and different stages of static CMOS logic, for various operating voltages & frequency.

It is clear that Energy Recovery logic dissipates the least power even at higher operating frequencies.

Conclusion

The use of electricity in high-speed, power-hungry circuits is thus made possible by Energy Recovery logic. This reasoning can be applied in memories to save power more effectively.

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