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Surveying Low Power VLSI Design Techniques: A Comprehensive Review

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A B S T R A C T

In the electronics industry of today, low power has become a major theme. For the design of VLSI chips, power dissipation has taken on equal importance to performance and area. The main issues below 100nm due to increased complexity are lowering power usage and overall power management on chip. Due to the requirement to lower package costs and increase battery life, power optimisation is crucial for many systems.

In low power VLSI designs, leakage current also has a significant impact on power management. An growing portion of integrated circuits' overall power dissipation is being accounted for by leakage current. This paper discusses numerous power management techniques, methodologies, and tactics for low power circuits and systems. Future challenges that must be met to designs low power high performance circuits are also discussed.

Keywords: Power Dissipation, Low Power, Process Nodes, Leakage Current, Power Management

Introduction

The benefit of combining low-power components with low-power design strategies is more important than ever before. As components get smaller, more battery-powered, and require more functionality, the need for lower power consumption is rising considerably. In the past, area, performance, and cost were the three main concerns for VLSI designers. The secondary problem was power consideration. Due to the extraordinary development and success of personal computers and wireless communication systems, which require high-speed computation and extensive functionality with minimal power consumption, power is now a major challenge. Application to application, many factors influence why power usage should be reduced. The objective is to maintain an appropriate battery lifetime, weight, and packaging cost for the category of micro-powered battery-operated portable applications, such as cell phones. The objective is to cut the power dissipation of the electronics component of the system to a level that is around half of the overall power dissipation for high performance portable computers like laptops. The general purpose of power minimization for high performance non-battery operated systems, like workstations, is to lower the system cost while ensuring long-term device reliability. Process technology has pushed power to the forefront of all elements in such designs for such high performance systems. Power consumption from leakage has joined switching activity as the main power management concern at process nodes with technology below 100 nm. Over the past ten years, a variety of strategies[15] have been created to address the continuously aggressive power reduction requirements of the majority of high performance. The fundamental methods of low power design, such as clock gating to cut down on dynamic power and multiple threshold voltage (multi-Vt) to cut down on leakage current, are well known and supported by current tools.[17] We may

analyse the number of changes in circuit design using Figure 1[15] by looking at power dissipation.

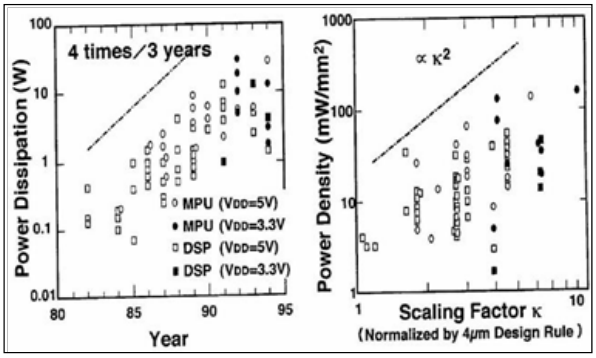

Figure 1.Evolution in Power dissipation[15]

Low Power Strategies

There (Table 1) are different strategies available at different level in VLSI design process for optimizing the power consumption:

Table 1

Design Level	Strategies
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit/Logic level	Logic styles, transistor sizingand energy recovery
Technology Level	Threshold reduction, multi thresholddevices

Effective power management is possible by using the different strategies at various levels in VLSI Design process. So designers need an intelligent approach for optimizing power consumptions in designs.

Power Dissipation Basics

In a circuit three components are responsible for power dissipation: dynamic power, short-circuit power and static power. Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below:[5,6]

$$P_{dynamic} = C_L Vdd^2 \alpha f \quad (1)$$

Where: CL: Load Capacitance, a function of fan-out, wire length, and transistor size; : Activity Factor, indicating how frequently the wires switch on average; f: Clock Frequency, increasing at each subsequent process node; Vdd: Supply Voltage; and f: Activity Factor. The supply voltage (Vdd), switching threshold (Vt), and transistor sizes all influence static power or leakage power (Figure 2). Leakage, which consumes at least 30% of total power,[2] becomes a more significant source of energy demand as process nodes get smaller. Crowbar currents, which happen when both NMOS and PMOS devices are turned on at the same time, also add to leaky power dissipation.[17] The majority of circuit level minimization strategies[15] solely consider sub threshold leakage reduction without taking gate leakage into account.For this reason, an MTCMOS technique[4] for lowering sub-threshold leakage current in sleep mode has been proposed. The many parts involved in power dissipation in CMOS are depicted in Figure 2.

From the above section it is revealed that there are three degrees of freedom in the VLSI design space : Voltage, Physical Capacitance and data activity. Optimizing for more power entails an attempt to reduce one or more of these factors.This section briefly describes about their importance in power optimization process.

Voltage

Because of its quadratic relationship to power, voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits andtechnologies, a factor of two reduction in supply voltage yields a factor of four decreases in power consumption. Unfortunately, there is speed penalty for supply voltage reduction and delays drastically increase as Vdd approaches to the threshold voltage Vt of the device. The approach to reduce the supply voltage without loss in throughput is to modify the threshold voltage of the devices. Reducing the Vt allows the supply voltage to be scaled down without loss in speed. The limit of how low low the Vt can go is set by the reqirement to set adequate noise margins and control the increase in the subtreshold leakage current.[6,8,10]

Table 2.Low power techniques used today[1,2]

Traditional Techniques	Dynamic Power Reduction	Leakage power reduction	Other Power reduction Techniques
Clock Gating	Clock Gating	Minimize usage of low Vt cells	Multi Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance
Variable Frequency	Variable Frequency	Back Biasing	Power circuits
Variable Voltage Supply	Variable Voltage Supply	Reduce Oxide Thickness	
Variable Device Threshold	Variable Island	Use FinFET	

Physical Capacitance

Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offer another technique for minimizing power consumption. The capacitances can be keptat a minimum by using less logic, smaller devices , fewer and shorter wires[6,8,10] As with voltage, however, we are not freeto optimize capacitances independently, for example reducing device sizes reduces physical capacitance, but it also reduces the current drive of the transistor making the circuit operate more slowly.

Switching Activity

There are two components to switching activity : F_{clk} which determines the average periodicityof data arrivals and E(sw) which determines how many transitions each arrival will generate.[14] E(sw) is reduced by selecting proper algorithms architecture optimization, by proper choice of logic topology and by logic level optimization which results in less power.[15] The data activity E(sw) are combined with the physical capacitance C to obtained switch capacitance C_{sw}=C.E(sw),which describes the average capacitance charge during each data period1/Fclk which determines the power consumed by CMOS circuit.[9]

Power Minimization Techniques

This section addresses (TABLE II) the different approaches to minimize the power at different levels:

Reducing Chip and package capacitance

This can be achieved through process development such as SOIwith partially or fully depleted wells, CMOS scaling to submicron device sizes and advanced interconnect substrates such as multi chip module (MCM). This approach can be very effective but is also very expensive.[15,19]

Scaling the supply voltage (Voltage Scaling)

This approach can be very effective in reducing the power dissipation, but often requires new IC fabrication processing. [13]

Using power management strategies

Effective power management involves selection of the right technology, the use of optimized libraries, IP (intellectual property), and design methodology.[1,19] Figure-3 shows the effective power management strategy.

The Role of Technology Selection: Proper technology selection is one of the key aspects of power management. [1] The goal of each technology advancement is to improve performance, density, and power consumption. The typical approach in developing a new generation of technology is to apply constant-electric-field scaling. Process designers scale both the applied voltage and the oxide thickness to maintain thesame electric field.[13,16] This approach reduces power by about 50% with every new technology node However, as the voltage gets smaller, the threshold voltage also must scale down to meet the performance targets of that technology. This scaling unfortunately increases the sub threshold current and hence the leakage power. To overcome this constraint, process engineers no longer apply constant-field scaling for processesof 65 nm or smaller; instead, they used a more generalized form of scaling. Because it is impossible to optimize a technology for both performance and leakage at once, each technology usually has two variants. One variant aims for high performance, and the other shoots for low leakage. The primarydifferences between the two are in the oxide thickness, supply voltage, and threshold voltage. The technology variant with the thicker gate oxide aims for low-leakage design and must support a higher voltage to achieve a reasonable performance

.[9]When selecting a technology to optimize the power for a given design, you must take both aspects into consideration: theneed to use a smaller geometry to reduce active power and the need to use a low-leakage variant to reduce leakage.

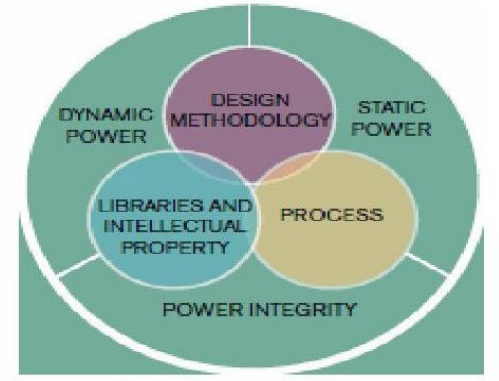

Figure3:Technologyselectionfor[9]effectivepowermanagement

Circuit-Design Techniques: After selecting technology, the focus is on design techniques to optimize power. (Figure 5). One has to start by selecting the appropriate logic gate from thestandard cell library. Each gate in a standard cell library uses the smallest transistors and has multiple versions with differentdrive strengths, sizes, delays, multiple-threshold voltage and power consumption. Because the main parameter for controlling active power is the power-supply voltage, cell designers typically design and characterize the gates to operate at voltages as much as 30% lower than the power-supply voltage.[1]

Figure4: Trade off between leakage and Power

Lowering the power-supply voltage produces smaller currents, resulting in more delay. However, this slowdown is acceptable if the design is not pushing the edges of a

given technology. Increasing the threshold voltage reduces the leakage current in the device. Leakage power also controlled by designing logic

gates with multiple-threshold-voltage devices,[16] including standard high and low threshold voltage devices. Figure-4 shows the variation of gate delay Vs leakage power.

CAD Methodologies and Technique: Today's EDA tools effectively support these power-management techniques.[3] They also provide additional power savings during implementation. Low power VLSI designs can be achieved at various levels of the design abstraction from algorithmic and system levels down to layout and circuit levels.

Table 3.Trade off associated with power managementtechniques

Power Reduction Technique	Power Benefit	Timing Penalty	Area Penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Multi Vt optimization	Medium	Little	Little	Low	Low	None	Low
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi supply voltage	Large	Some	Little	High	Medium	Low	Medium
Power Shut off	Huge	Some	Some	High	High	High	High
Dynamic and adaptive Voltage frequencyscaling	Large	Some	Some	High	High	High	High
SubstrateBiasing	Large	Some	Some	Medium	None	None	High

Low Power management in Physical Design

Physical design tools interpret the power intent and implement the layout correctly, from placement of special cells to routing and optimization across power domains in the presence of multiple corners, modes, and power states, plus manufacturing variability.[2,3] An increasingly common technique to reduce power in physical design is the use of multiple voltage islands (domains), which allows some blocks to use lower supply voltages than others, or to be completely shut off for certain modes of operation.[6] Clocks are a significant source of dynamic power usage. Low-power clock tree synthesis (CTS) strategies[5,6] include lowering overall capacitance and minimizing switching activity to achieve power saving. However, getting the best power results from CTS depends on

the ability to synthesize the clocks for multiple corners and modes concurrently in the presence of design and manufacturing variability, and in multi-voltage flows.[8] Power gating technique is effective for reducing leakage power by temporarily turned off the circuit.[17,8]

This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required foroperation once again they are activated to "active mode". Shutting down the blocks can be accomplished either by software or hardware. Now-a-days a dedicated power. management controller is used for this purpose.[17] Table-3 gives the trade-off associated with the various power management techniques.[17]

Conclusion

Numerous market segments are pushing for lower power solutions. Unfortunately, designing for low power adds still another layer to the already challenging design problem, necessitating power as well as performance and area optimisation. In conclusion, a number of problems and significant difficulties with low power designs are:Scaling Technology to One: The following parameters are related to it: Die size grows by 14% (Moore's Law), Capacitance per node decreases by 30%, Electrical nodes expand by 2X, Supply Voltage decreases by 15%, and Frequency increases by 2X. Relatively 2.7 X more active power will be added to address these problems. 2 Leakage power: Vt will be scaled to match frequency requirements, which leads to excessive leakage power. a low voltage/low threshold technology and circuit design strategy that aims for supply voltages of roughly 1V and operates at lower thresholds.

3 Dynamic power management strategies, with supply voltage and execution speed adjusted for activity monitoring.

4 Low power connectivity, low swing or activity approach, using advanced technology.

5 Creation of power-conscious methods and tools for layout optimisation, behavioural synthesis, and logic synthesis.

In some situations where speed can be exchanged for low power, adiabatic switching approaches that recycle signal energy instead of dispersing them as heat show promise.

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