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Research Article

A Low Power Translinear based CMOS Analog Multiplier

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A B S T R A C T

In this work, a novel technique for creating four-quadrant CMOS analogue multipliers has been introduced. The main part of the proposed multiplier circuit, which is symmetrically arranged, is composed of a cascode current source and two common pairs of translinear loops. This symmetrical design reduces error by subtracting the resultant error in two square circuits from one another. Additionally, the shared bias branch of the multiplier circuit consumes less power than traditional designs, as both squarer circuits share a single bias branch rather than having two separate ones. For 180 nm technology, the circuit operates with a maximum power consumption of 92.34 µW, a bandwidth of 722 MHz (-3 dB), and a maximum supply voltage of 1.5 V.

Keywords: Power consumption, Low voltage, Translinear loop, FGMOS

Introduction

Four-quadrant multipliers are essential in analog signal processing systems. These multipliers are vital for various electronic circuits, including automatic gain control. Their applications, such as modulation, neural networks, phase-locked loops (PLL), frequency conversion, mixers, and fuzzy systems, are well-documented in the literature[1]. Under ideal circumstances, the output of an analog multiplier is characterized by the linear multiplication of the two input signals, x and y. This multiplication yields an output signal of z = Kxy, where K represents a constant value. Multiplier circuits are categorized based on their performance characteristics. When the inputs x and y are non-polarized, a one-quadrant circuit is formed. In cases where only one of the two input signals is polarized, a two-quadrant circuit is formed[2-4]. Furthermore, if both input signals are polarized, a four-quadrant circuit is formed[4].

The Translinear (TL) loop method is utilized to develop a significant group of multipliers in the current mode[3-5]. A TL loop arranges the transistors in a specific configuration within the loop, allowing for a strong signal connection for the transistor currents[6-8]. A notable advantage of these circuits is that the output current remains unaffected by variations in transistor characteristics, ensuring design stability even under changing temperatures.

This work introduces a novel topology for creating analog multiplier circuits based on Tran's linear loops, using a regulated cascade current mirror. The fundamental components of a CMOS analog multiplier circuit are two common pairs of Tran's linear loops. By employing a unique method of sharing a bias branch among the Translinear loops, the proposed circuit achieves reduced power consumption. Additionally, the circuit features a wide bandwidth and is immune to body effect. While cascading is a widely used technique to increase output resistance and DC gain, it is not ideal for low-voltage analog circuits because it can only

stack up to two transistors due to limited supply voltage. To mitigate the impact of channel length modulation, the drain-source voltage (Vds1) of M_1 is stabilized at a constant value using a feedback loop. This feedback loop includes an auxiliary amplifier made up of M3and current source Ib, with M_2 functioning as a source follower. This approach enhances the output resistance and DC gain of the circuit, resulting in improved overall performance.

Materials & Methods

Design of Circuit

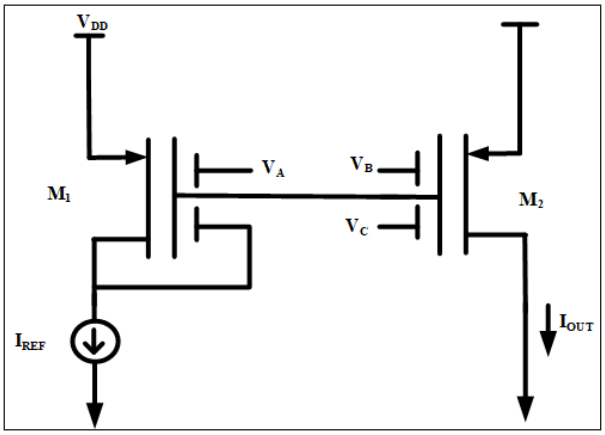

Figure 1.Current Mirror[1]

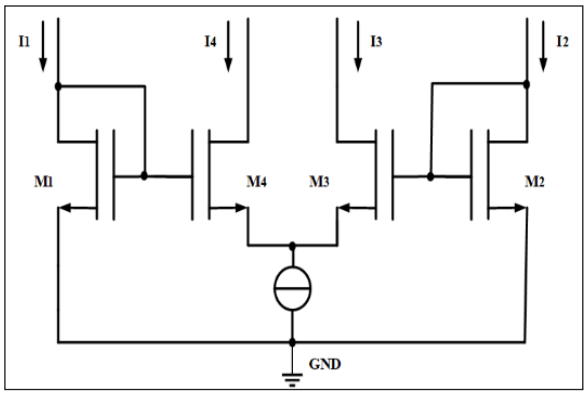

Figure 2 Translinear Loop Circuit[5]

The current mode squaring circuit

Fig. 3.show the proposed current squaring circuit. This circuit consists of two dual Translinear loop (TL). The first TL is transistors , , , and , while the second TL incorporates transistors , , , and .

Here and is FGMOS[7] (Floating Gate MOS). The following equation may be obtained from the fact that every MOS transistor operates in the saturation region:

$I_{DS}= (V_{GS}-V_T)^2$ ... (1)

Where $K_1= 0.5_0C_{OX}$ (W/L).

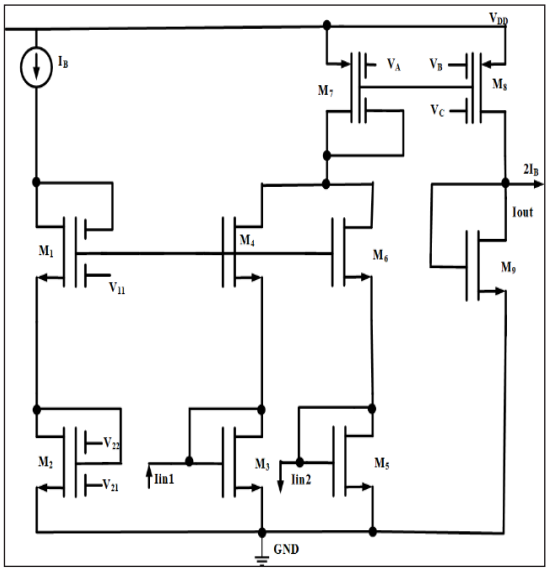

Figure 3.The proposed FGMOS based squarer circuit design

The multiplier circuit

The proposed analog Multiplier's working principle is based on the following algebraic structure: $(x+y)^2-(x-y)^2=4xy$ ... (2)

The output of is obtained from the first loop, consisting of transistors,,, and, while the output of is provided by the second TL, both loops share transistors and. In contrast to previous approaches that duplicated this branch for the loops and utilized a normal current mirror instead of a regulated cascode current mirror, this innovative method significantly reduces power consumption in the circuit, resulting in comparatively lower power dissipation.

The overall circuit functionality is:

$$I_{01} = \frac{I_{in1}^2}{8I_B} \quad \ldots (3)$$

$$I_{02} = \frac{I_{in2}^2}{8I_B} \quad \ldots (4)$$

$$I_{out} = I_{02} - I_{01} \quad \ldots (5)$$

Since, and

$$I_{in1} = I_x - I_y \text{and} I_{in2} = I_x + I_y \quad \ldots (6)$$

$$\mathrm{I_{out}} = \frac{\mathrm{I_X I_Y}}{2\mathrm{I_B}}$$

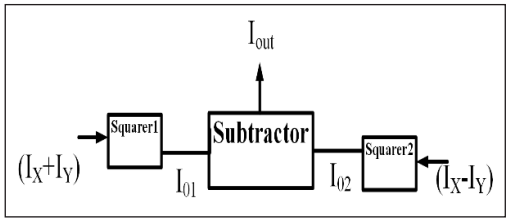

Figure 4.Block diagram of Proposed Multiplier

The output of the proposed multiplier circuit, depicted in equation (6) is obtained by dividing the product of the two inputs by the constant current, which has a fixed value of 10 µA.

Results and Discussion

Discussion Results

Figure 1 and Figure 2 depict the current mirror and the translinear loop circuit, respectively. The proposed circuit was designed and simulated using the Cadence EDA tool with 180 nm CMOS technology, as shown in Figure 3. The circuit operates with a power supply of 1.5V, and the bias current IB is set to 10 µA. Figure 4 shows the block diagram of the multiplier. Figure 5 shows the DC analysis of the proposed current squarer, where a triangular input current with an amplitude of 15 µA at 1 MHz results in an output current of 3.3125 µA. Figure 6 shows the transient power dissipation of the proposed squarer circuits. Figure 7 presents the DC analysis of the proposed multiplier. This current mirror-based squarer notably demonstrates a 30% reduction in power consumption compared to previous works. The power consumption of the squarer is illustrated based on variations in different technologies, showing approximately a 30% reduction in power dissipation and a 3 dB increase in bandwidth.

Simulation Results

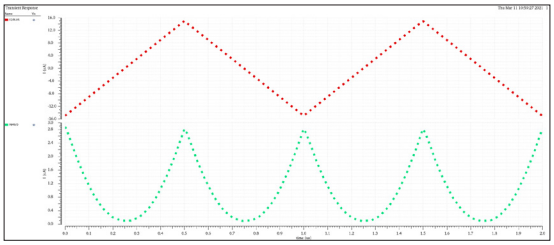

Figure 5.Input-output wave form of squarer

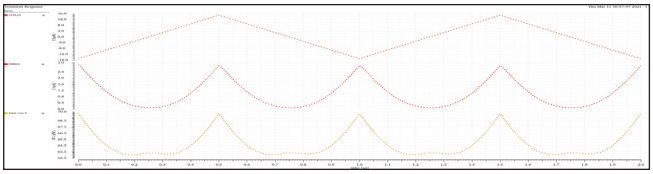

Figure 6.Transient Power

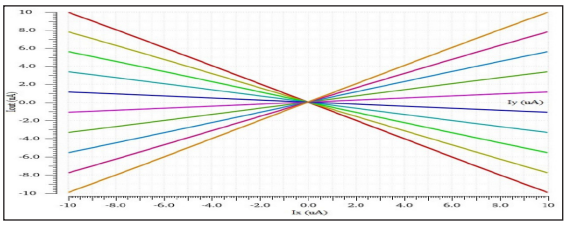

Figure 7.DC analysis of Multiplier

Conclusion

In this work novel LV and LP, MOS transistors and translinear-based current-mode analogue squarers are successfully implemented. This circuit is designed based on an MOS transistor and two TL loops. The MOS transistor-based current mirror is utilised in this circuit, and MOS has the capability to reduce threshold voltage, and current copying is also extremely efficient. As a result, the power consumption of the squarer circuit is reduced. It has a number of benefits, including reduced power consumption, low voltage requirements, high accuracy and wide bandwidth, as compared to the previous works. Here input current is -15 µA to 15 µA. It is used as a modulator and a frequency doubler. The proposed multiplier's low power and efficiency were demonstrated by a comparison with earlier works.

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